IN THE SPECIFICATION

Please replace the paragraph beginning at line 14, page 5 with the following rewritten paragraph:

--Figure 2 is a high-level flow chart of one embodiment of a method 200 in accordance with the present invention for providing a semiconductor device having self aligned contacts with a lower sheet resistance. The semiconductor device has a core and a periphery, which are fabricated on a substrate. A plurality of core gate stacks in the core, via step 202. Each of the plurality of core gate stacks includes a first polysilicon gate and a WSi layer above the first polysilicon gate. Consequently, electrical contact can be made to the first polysilicon gate. In a preferred embodiment, spacers will also be formed at the edges of the core gate stacks.--

Please replace the paragraph beginning at line 14, page 6 with the following rewritten paragraph:

--A first layer of polysilicon that will be used in forming gates and a protective layer are provided over a substrate 101 in both a core region 102 and a periphery 104, via step 212. Figure 4A depicts the semiconductor device 100 after formation of the polysilicon layer 152 and the protective layer 154. The protective layer 154 is preferably made of SiN, SiON or an oxide. The portion of the protective layer that is over the core is then removed to open the core, via step 214. Preferably, step 214 includes providing a photoresist mask that has an aperture over the core 102 and covers the periphery 104. Figure 4B depicts the semiconductor device 100 after step 214 is completed. The polysilicon layer 152 is exposed over the core 102, with a remaining portion 154' of the protective layer residing over the periphery 104.--